EXHIBIT 1

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC., Defendant.	)	C.A. No. 13-cv-1835-RGA **PUBLIC VERSION**

DEFENDANT 2WIRE, INC.'S OPENING BRIEF IN SUPPORT OF ITS MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF THE ASSERTED CLAIMS OF U.S. PATENT NOS. 8,276,048; 7,836,381; 7,844,882; AND 8,495,473 ("FAMILY 3")

Dated: February 22, 2019

Brett Schuman (*pro hac vice*)
Rachel M. Walsh (*pro hac vice*)
Monte M.F. Cooper (*pro hac vice*)
GOODWIN PROCTER LLP
Three Embarcadero Center, 24th Floor
San Francisco, California 94111
Telephone: 415.733.6000
bschuman@goodwinprocter.com
rwalsh@goodwinprocter.com
mcooper@goodwinlaw.com

Jody C. Barillare (#5107)
MORGAN LEWIS & BOCKIUS LLP
The Nemours Building
1007 North Orange Street, Suite 501
Wilmington, Delaware 19801
Telephone: 302.574.3000
jody.barillare@morganlewis.com

Attorneys for Defendant 2Wire, Inc.

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Page(s)

Cases

Statutes

Other Authorities

I. SUMMARY OF THE ARGUMENT

2Wire, Inc. ("2Wire") is entitled to summary judgment that none of the Accused 2Wire Products infringe the asserted claims of the Family 3 patents for at least the following reasons.[1]

First, for claim 1 of the '048 patent, claim 5 of the '381 patent, and claim 13 of the '882 patent, the Accused 2Wire Products do not transmit or receive "a message during initialization specifying a maximum number of bytes of memory that are available to be allocated" to an interleaver or deinterleaver.

Broadcom, the supplier of the DSL chips that control the DSL functionality in all of the Accused 2Wire Products, has testified that none of the products transmit or receive the claimed message during initialization.

To try to prove infringement, TQ Delta's experts, Dr. Cooklev and Dr. Almeroth, rely upon two parameters from ITU-T Recommendation G.993.2, max_delay_octet$_{DS,0}$ and max_delay_octet$_{US,0}$, that specify only the maximum allowed end-to-end ***delay*** between an interleaver and deinterleaver for a particular latency path. By specifying the maximum allowed delay, these parameters enable the receiving transceiver to determine the opposite of what is required by the claims—the *minimum* amount of interleaver or deinterleaver memory that is needed to support the maximum end-to-end delay. There is no message specifying the maximum number of bytes of memory available to be allocated, as claimed.

Second, for claim 19 of the '473 patent, the Accused 2Wire Products do not allocate memory "in accordance with a message received during an initialization of the transceiver." Although this claim language is different than the language in the other asserted claims, TQ

[1] TQ Delta accuses 2Wire's 5031NV, 5168NV, and i3812V products (the "Accused 2Wire Products") of infringing claim 1 of U.S. Patent No. 8,276,048 (the "'048 patent"), claim 5 of U.S. Patent No. 7,836,381 (the "'381 patent"), claim 13 of U.S. Patent No. 7,844,882 (the "'882 patent"). TQ Delta only accuses 2Wire's model 5031NV and 5168NV DSL transceivers of infringing claim 19 of U.S. Patent No. 8,495,473 (the "'473 patent").

Delta relies on the same theory and same purported evidence to try to prove infringement. TQ Delta's approach fails here, too, as explained below. Additionally, claim 19 of the '473 patent requires that the memory "***is*** allocated" based on a received message, which only occurs during operation of the accused products. 2Wire does not operate DSL networks and, for this additional reason, it does not infringe claim 19 of the '473 patent.

Third, and in addition to the reasons listed above, for claim 5 of the '381 patent and claim 13 of the '882 patent, it is undisputed that none of the Accused 2Wire Products practice the limitations of "allocating a first number of bytes of the shared memory to the deinterleaver . . ." and "allocating a second number of bytes of the shared memory to the interleaver . . ." as those limitations read when the patents issued. After the patents issued, the applicants obtained certificates of correction that materially changed the scope of the claims. The Court should invalidate the certificates under 35 U.S.C. § 255. Once the certificates of correction are invalidated, as 2Wire requests here, it is undisputed that none of the Accused 2Wire Products infringe these claims.

II. NATURE AND STAGE OF THE PROCEEDINGS

TQ Delta filed this patent infringement lawsuit against 2Wire over five years ago on November 3, 2013, asserting infringement of twenty-four patents across six patent families. *See* D.I. 1, D.I. 7 (Complaint, and First Amended Complaint, respectively). The Court split the case into separate trials on individual patents families. *See* D.I. 280 (Third Amended Scheduling Order). Family 3 is currently at issue, and TQ Delta asserts claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the'882 patent, and claim 19 of the '473 patent.

Fact and expert discovery is closed. A pretrial conference for 2Wire's trial on Family 3 is set for May 10, 2019, and trial is set for May 20, 2019. *See* D.I. 513 (Final Scheduling Order).

III. FACTUAL BACKGROUND

A. The Family 3 Patents.

The claims of the Family 3 patents are directed to methods, systems, and apparatuses for allocating shared memory between transmitter and receiver latency paths. *See* Cooper Decl., Ex. C ('882 patent) at 4:1–3.[2] The transmitter and receiver latency paths can share an interleaver/deinterleaver memory, which can be allocated to the transmitter's interleaver and to the receiver's deinterleaver. *Id.* at 4:5–9, 9:18–21.

The Family 3 patents provide an example in which a first transceiver sends a message to a second transceiver indicating the number of supported transmitter and receiver latency paths, the maximum interleaver memory for each of the latency paths, and the maximum total or shared memory for all of the latency paths. *Id.* at 8:9–19. The first transceiver then selects settings (i.e., Reed-Solomon parameter values N and R, and the interleaver depth, D) for each of the latency paths. *Id.* at 8:21–22.

1. Asserted Claims.

Claim 1 of the '048 patent, claim 5 of the '381 patent, and claim 13 of the '882 patent are all similar and recite as follows:[3]

'048 Patent, Claim 1	'381 Patent, Claim 5	'882 Patent, Claim 13
1. A system that allocates shared memory comprising: a transceiver that is capable of:	5. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:	13. A system that allocates shared memory comprising: a transceiver that performs:
transmitting or receiving a	transmitting or receiving, by	transmitting or receiving a

[2] The Family 3 patents share a common specification and have the same drawings. References to the specification herein will be to the '882 patent.

[3] Claim 5 of the '381 patent and claim 13 of the '882 patent have the edits set forth in the February 8, 2011 and May 3, 2011 certificates of correction, respectively.

message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;	the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;	message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;
determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;	determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;	determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;
allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;	allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ~~transmission~~ [reception] at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;	allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ~~transmission~~ [reception] at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;
allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and	allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes ~~received~~ [transmitted] at a second data rate; and	allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes ~~received~~ [transmitted] at a second data rate; and
interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared	deinterleaving the first plurality of RS coded data bytes within the ~~shred~~ [shared] memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared	deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the ~~shred~~ [shared] memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the

memory allocated to the deinterleaver.	memory allocated to the interleaver.	shared memory allocated to the interleaver.

Claim 19 of the '473 patent recites:

19. An apparatus comprising:

a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path, the multicarrier communications transceiver being associated with a memory,

wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

2. Claim Construction.

The Court issued claim constructions for certain terms in the asserted claims of the Family 3 patents. D.I. 294 (Claim Construction Order). The constructions that are potentially relevant to this motion are as follows:

Term or Phrase	Court's Construction
"shared memory"	"common memory used by at least two functions, where a portion of the memory can be used by either one of the functions"
"the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]	"the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory"
"latency path"	"transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay"
"portion of memory"	plain meaning
"memory is allocated between the [first] interleaving function and the [second interleaving / deinterleaving] function"	"an amount of the memory is allocated to the [first] interleaving function and an amount of memory is allocated to the [second interleaving / deinterleaving] function"

B. Interleaving Delay and Memory as Specified in G.993.2.

Even though it does not contend that any of the Family 3 patents are SEPs, TQ Delta relies on messages specified in the ITU-T's G.993.2 Recommendation, known as "VDSL2," to try to prove infringement. G.993.2 concerns interleaving and forward error connection (FEC), and the exchange of information associated with interleaving and FEC (specifically, Reed-Solomon coding). *See* Jacobsen Decl. ¶¶ 88–104; Cooper Decl., Ex. E (G.993.2) at i.

Considering the simplest VDSL2 configuration, which uses only a single downstream latency path and a single upstream latency path, the maximum end-to-end interleaver delay constraints, in octets, are given by the values of $\text{max\_delay\_octet}_{DS,0}$ for the downstream direction and $\text{max\_delay\_octet}_{US,0}$ for the upstream direction. *See* G.993.2 § 12.3.5.2.1.3. The value of $\text{max\_delay\_octet}_{DS,0}$ is the maximum allowed end-to-end delay, in octets, that can result from the combination of the VTU-O's configured interleaver and the VTU-R's configured deinterleaver for downstream latency path zero.[4] *Id.* Likewise, $\text{max\_delay\_octet}_{US,0}$ is the maximum allowed end-to-end delay, in octets, that can result from the combination of the VTU-R's configured interleaver and the VTU-O's configured deinterleaver for upstream latency path zero. *Id.* The VTU-O sends the selected values of $\text{max\_delay\_octet}_{DS,0}$ and $\text{max\_delay\_octet}_{US,0}$ to the VTU-R during the VDSL2 initialization procedure in a message called "O-PMS." *Id.*

The actual end-to-end interleaver delays, in octets, of the downstream and upstream latency paths, which are the delays that result from the selected interleaving parameters *I* (block length) and *D* (interleaver depth), are denoted by the parameters $\text{delay\_octet}_{DS,0}$ (for latency path zero in the downstream direction) and $\text{delay\_octet}_{US,0}$ (for latency path zero in the upstream

[4] In VDSL, the transceiver located on the service provider's side of the subscriber line is referred to as the "VTU-O," and the transceiver located on the customer's side of the subscriber line is referred to as the "VTU-R." Jacobsen Decl. ¶ 51. The direction of transmission from the VTU-O to the VTU-R is referred to as the *downstream* direction, and the direction of transmission from the VTU-R to the VTU-O is referred to as the *upstream* direction. *Id.* ¶ 52.

direction). *Id.* at § 6.2.8. Specifically, $\text{delay\_octet}_{DS,0} = (I_{DS,0} - 1) \times (D_{DS,0} - 1)$ and $\text{delay\_octet}_{US,0} = (I_{US,0} - 1) \times (D_{US,0} - 1)$, where $I_{DS,0}$ and $D_{DS,0}$ are, respectively, the interleaver block length and depth for latency path zero in the downstream direction, and $I_{US,0}$ and $D_{US,0}$ are, respectively, the interleaver block length and depth for latency path zero in the upstream direction. *Id.* The value of $\text{max\_delay\_octet}_{DS,0}$ is the maximum allowed value of the parameter $\text{delay\_octet}_{DS,0}$. *Id.* at § 12.3.5.2.1.3. And the value of $\text{max\_delay\_octet}_{US,0}$ is the maximum allowed value of the parameter $\text{delay\_octet}_{US,0}$.

G.993.2 states that the ***minimum amount*** of memory the VTU-O or the VTU-R must use to meet each of the delay_octet values is half of the specified delay. *Id.* § 6.2.8 ("Each interleaver and each de-interleaver for each latency path requires ***at least*** $(\text{delay\_octet}_{[DS/US],[0]}/2)$ octets of memory to meet this delay.") (emphasis added). Thus, the values of $\text{delay\_octet}_{DS,0}$ and $\text{delay\_octet}_{US,0}$ establish only lower bounds on the amounts of memory that the VTU-R and VTU-O must actually use for interleaving and deinterleaving.

IV. LEGAL STANDARD

Summary judgment is appropriate where the record, read in the light most favorable to the non-moving party, indicates that "there is no genuine issue as to any material fact and . . . the moving party is entitled to a judgment as a matter of law." Fed. R. Civ. P. 56(c). A patent owner has the burden of proving infringement by showing that every limitation of the asserted claims is found in the accused device and must meet its burden by a preponderance of the evidence. *See SmithKline Diagnostics, Inc. v. Helena Lab. Corp.*, 859 F.2d 878, 889 (Fed. Cir. 1988). The absence of even one claim limitation "is sufficient to negate infringement." *Kraft Foods, Inc. v. Int'l Trading Co.*, 203 F.3d 1362, 137 (Fed. Cir. 2000).

V. ARGUMENT

A. It Is Undisputed That The Accused 2Wire Products Do Not Transmit Or Receive Any "Message During Initialization Specifying A Maximum Number Of Bytes Of Memory That Are Available To Be Allocated" To An Interleaver Or Deinterleaver.

No reasonable jury could conclude that the Accused 2Wire Products transmit or receive "a message during initialization specifying a maximum number of bytes of memory that are available to be allocated" to an interleaver or deinterleaver as set forth in claim 1 of the '048 patent, claim 5 of the '381 patent, and claim 13 of the '882 patent. *See* Jacobsen Decl. ¶ 163. Therefore, 2Wire is entitled to summary judgment of non-infringement.

1. Broadcom Has Testified That The Accused Products Do Not Infringe.

The DSL functionality in all of the Accused 2Wire Products is undisputedly controlled by DSL chips supplied by Broadcom. TQ Delta took Broadcom's deposition. Dr. Gong-San Yu, Broadcom's Rule 30(b)(6) designee on the operation of the Broadcom chips, testified that none of the Accused 2Wire Products send or receive "a message specifying a maximum amount of memory available to be allocated" to an interleaver or deinterleaver as required by the claims:

Claim Limitation	Accused Product	Citation to 5/23/18 Yu Dep. Tr.
'048 patent, claim 1: "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver"	5168NV, which uses the BCM 63168 chipset	[redacted] Walsh Decl., Ex. E (5/23/18 Yu Dep. Tr.) at 443:20–24. [redacted] *Id.* at 444:8–12.
	5031NV, which uses the BCM 6368 chipset	[redacted] *Id.* at 446:13–17. [redacted]

Claim Limitation	Accused Product	Citation to 5/23/18 Yu Dep. Tr.
’381 patent, claim 5; and ’882 patent, claim 13: “transmitting or receiving[, by the transceiver,] a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver”	i3812V, which uses the BCM 6091 chipset	[redacted] *Id.* at 447:24–448:3. [redacted] *Id.* at 452:9–13. [redacted] *Id.* at 453:9–13.
	5168NV, which uses the BCM 63168 chipset	[redacted] *Id.* at 444:2–6. [redacted] *Id.* at 444:14–18.
	5031NV, which uses the BCM 6368 chipset	[redacted] *Id.* at 446:19–23. [redacted] *Id.* at 448:5–9.
	i3812V, which uses the BCM 6091 chipset	[redacted] *Id.* at 452:15–19. [redacted] *Id.* at 453:15–19.

This evidence is undisputed, and it is sufficient to carry 2Wire’s moving-party burden of producing evidence of non-infringement. *See Novartis Corp. v. Ben Venue Labs., Inc.*, 271 F.3d 1043, 1046 (Fed. Cir. 2001).

2. Dr. Cooklev's Opinions Relating To G.993.2 Do Not Create Any Genuine Disputes Of Material Fact.

Dr. Cooklev's opinions relating to G.993.2 do not create any genuine dispute of material fact sufficient to preclude entry of summary judgment of non-infringement. Dr. Cooklev's reliance upon parameters from G.993.2—max_delay_octet$_{DS,0}$ and max_delay_octet$_{US,0}$—does not establish that the Accused 2Wire Products transmit or receive "a message during initialization specifying a maximum number of bytes of memory that are available to be allocated" to an interleaver or deinterleaver.

In his opening expert report, Dr. Cooklev correctly states that:

> For use cases where a single latency path is being used in the upstream direction and a single latency path is being used in the downstream direction, "max_delay_octetDS,0" in field #8 of the O-PMS message specifies the maximum delay for the VTU-O interleaver/VTU-R deinterleaver, and "max_delay_octetUS,0" in field #10 of the O-PMS message specifies the maximum delay for the VTU-R interleaver/VTU-O deinterleaver. *See id.* at pp. 245-246. The parameter values max_delay_octetDS,0 and max_delay_octetUS,0 are specified in bytes. *Id.* at p.246.

Walsh Decl., Ex. A (Cooklev Opening Rpt.) ¶ 101. However, Dr. Cooklev then states: "Per the VDSL2 standard, the maximum number of bytes of VTU-R deinterleaver memory is specified as one-half of max_delay_octet$_{DS,0}$ and the maximum number of bytes of VTU-R interleaver memory is specified as one-half of max_delay_octet$_{US,0}$." *Id.* This is where Dr. Cooklev errs.

As discussed above, in G.993.2, max_delay_octet$_{DS,0}$ and max_delay_octet$_{US,0}$ set forth the maximum allowed end-to-end ***delay*** between an interleaver and deinterleaver for a particular latency path. *See* Jacobsen Decl. ¶ 94. G.993.2 separately specifies that the minimum amount of memory required to meet each of the delay_octet values, as constrained by max_delay_octet, is ½ of the specified delay. *Id.* ¶¶ 99–100; G.993.2 § 6.2.8 ("Each interleaver and each de-interleaver for each latency path requires ***at least*** (delay_octet$_{[DS/US],[0]}$/2) octets of memory to meet this delay") (emphasis added). In other words, the values of max_delay_octet$_{DS,0}$ and

max_delay_octet$_{US,0}$ establish only the minimum amount of memory that the VTU-R and VTU-O must actually use to support the maximum end-to-end delay. *See also* G.993.2 § 6.2.8 ("The ***minimum amount of memory required*** in a transceiver (VTU-O or VTU-R) to meet this requirement is MAXDELAYOCTET/2 octets.") (emphasis added); Jacobsen Decl. ¶¶ 103–04.

In sum, max_delay_octet$_{DS,0}$ and max_delay_octet$_{US,0}$ do not specify a maximum amount of memory to be used by an interleaver or deinterleaver, nor do they specify the actual amount of memory used. The variables relied upon by TQ Delta's experts thus do not create a triable issue of material fact that the accused products transmit or receive "a message during initialization specifying a maximum number of bytes of memory that are available to be allocated."

3. Dr. Cooklev's Testing Is Insufficient To Create Any Genuine Disputes Of Material Fact.

Dr. Cooklev's testing of the Accused 2Wire products, conducted by a third party under Dr. Cooklev's direction, also does not create any genuine disputes of material fact. *See* Cooklev Opening Rpt. ¶¶ 167–212. In his tests, Dr. Cooklev sought "to determine if each of the representative Accused Products receives, during the channel analysis and exchange phase of initialization, the O-PMS message from a CO modem, as set forth in the VDSL2 standard." *Id.* ¶ 173. But, the O-PMS message simply provides the maximum allowed end-to-end delay, in the form of max_delay_octet$_{DS,0}$ and max_delay_octet$_{US,0}$. *See* Jacobsen Decl. ¶¶ 182–85. These parameters do not specify the maximum amount of memory to be allocated, so it is irrelevant that Dr. Cooklev was able to confirm receipt of the O-PMS message. *Id.*

a. Dr. Cooklev's Test Methodology.

For each product, Dr. Cooklev used two configurations, which he refers to as the "60/20 Configuration" (60 Mbit/s downstream, 20 Mbit/s upstream) and the "50/50 Configuration" (50 Mbit/s downstream and 50 Mbit/s upstream). *See* Cooklev Opening Rpt. ¶¶ 185–86.

For claim 1 of the '048 patent and claim 19 of the '473 patent, Dr. Cooklev's approach was to (a) determine the value of max_delay_octet$_{DS,0}$ received by the 2Wire Accused Product in the O-PMS message, (b) extract the values of *I* and *D* for the downstream latency path from the R-PMS message transmitted by the 2Wire Accused Product, (c) calculate $(I-1)(D-1)/2$ using the values from the R-PMS message, and (d) compare the value of $(I-1)(D-1)/2$ to one-half of the value of max_delay_octet$_{DS,0}$ received in the O-PMS message. *See, e.g.*, *id.* ¶¶ 326–331; *see also* Jacobsen Decl. ¶ 180. Dr. Cooklev's approach for claim 5 of the '381 patent and claim 13 of the '882 patent was similar: (i) determine the value of max_delay_octet$_{US,0}$ received by the 2Wire Accused Product in the O-PMS message, (ii) extract the values of *I* and *D* for the upstream latency path from the O-PMS message received by the 2Wire Accused Product, (iii) calculate $(I-1)(D-1)/2$ using the values from the O-PMS message, and (iv) compare the value of $(I-1)(D-1)/2$ to one-half of the value of max_delay_octet$_{US,0}$ received in the O-PMS message. *See, e.g.*, Cooklev Opening Rpt. ¶¶ 239–45, 422–28; *see also* Jacobsen Decl. ¶ 180.

For each of his tests, Dr. Cooklev concluded that the value of $(I-1)(D-1)/2$ (i.e., the calculated value of delay_octet) was less than the value of max_delay_octet specified in the O-PMS message. *See* Cooklev Opening Rpt. ¶¶ 243–44, 330–31, 426–27. These results are unsurprising given the specifications of G.993.2: max_delay_octet identifies the maximum amount of actual end-to-end delay, delay_octet. However, as above, the parameters provide no information regarding the actual amount of memory used by the interleaver or deinterleaver in achieving the end-to-end delay, as required by the claims. *See* Jacobsen Decl. ¶¶ 181–85.

b. Dr. Cooklev's Misinterpretation Of His Test Results.

Dr. Cooklev's misinterpretation of his test results is rooted in his misunderstanding of the O-PMS message, and the parameters specified by it, as discussed above.

For example, in his 50/50 configuration test for the 5031NV, Dr. Cooklev states that [redacted] *Id.* Not so. As already explained above, the values of I and D are used to calculate the actual end-to-end delay (through the equation $(I - 1) \times (D - 1)$), and ½ of this actual end-to-end delay simply indicates the *minimum amount* of memory required to support that delay. *See* Jacobsen Decl. ¶¶ 93, 99.

For the same test, Dr. Cooklev opines that, [redacted] Cooklev Opening Rpt. ¶ 243. Dr. Cooklev's conclusion here is also incorrect. [redacted]

[redacted] *Id.*

Dr. Cooklev applies this same flawed analysis to each of the test configurations (50/50 and 60/20) that he used for each of the Accused 2Wire Products. *Id.* ¶¶ 201–02, 221–23, 240–44, 268–70. Thus, Dr. Cooklev's test results do not establish that the Accused 2Wire specify the "maximum number of bytes of memory that are available to be allocated."

4. Dr. Almeroth's Opinions Based On His Source Code Review Do Not Create Any Genuine Disputes Of Material Fact.

Dr. Almeroth's source code analysis, which is based on the same misunderstanding of G.993.2 as Dr. Cooklev's opinions, is insufficient to defeat summary judgment.

For each of the accused products, Dr. Almeroth states that a function in the firmware code [redacted] *See, e.g.*, Walsh Decl., Ex. F (Almeroth Opening Rpt.), Attachment F at 7, Attachment I at 7, Attachment J at 7. Based on this piece of code, Dr. Almeroth concludes that [redacted] *Id.*, Attachment F at 6. Dr. Cooklev draws a similar conclusion. *See* Cooklev Rpt. ¶¶ 246, 333, 516. Dr. Cooklev and Dr. Almeroth are both wrong.

Dr. Almeroth actually reversed his opinion at his Family 3 deposition. There, he admitted that the max_delay_octet parameters ***do not*** specify the maximum amount of memory allocated to an interleaver or deinterleaver:

[redacted]

Walsh Decl., Ex. G (2/8/19 Almeroth Dep. Tr.) at 196:10–18 (emphasis added).

Dr. Almeroth's deposition admission that [redacted]

[redacted] is consistent with the definitions of these parameters in G.993.2, described above. In short, even if each of the Accused 2Wire Products receives an O-PMS message and [redacted] as Dr. Almeroth stated in his report, those values do not specify a maximum number of bytes of memory that are available to be allocated to a deinterleaver or to an interleaver, as required by the asserted claims. *See* Jacobsen Decl. ¶¶ 203, 224. Instead, one-half of each of those variables merely provides the minimum amount of deinterleaver or interleaver memory necessary to support the maximum end-to-end delay. *Id.* ¶¶ 99–103.

B. The Accused 2Wire Products Do Not Infringe Claim 19 Of The '473 Patent.

No reasonable jury could conclude that the Accused 2Wire Products allocate memory "between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver" as required for claim 19 of the '473 patent. *See* Jacobsen Decl. ¶ 164. TQ Delta's evidence of infringement fails to create a triable issue of material fact that this limitation is met. In addition, claim 19 requires that "the memory ***is allocated*** between the interleaving function and the deinterleaving function in accordance with a message ***received during an initialization*** of the transceiver . . . ." This allocation of memory can only occur, if it occurs at all, when the Accused 2Wire Products are installed by a DSL service provider in a network and after the VTU-R receives a message from the VTU-O. 2Wire does not put the Accused 2Wire Products into operation and therefore cannot infringe claim 19.

1. The Accused 2Wire Products Do Not Allocate Memory "Between the Interleaving Function and the Deinterleaving Function in Accordance With a Message Received During an Initialization of the Transceiver."

Although claim 19 of the '473 patent is a little different than the other asserted Family 3 claims (*e.g.*, claim 19 does not recite a message during initialization specifying a maximum number of bytes of memory that are available to be allocated), TQ Delta and Dr. Cooklev rely on

the same flawed arguments and evidence to try to prove infringement of this claim as they do with respect to the other asserted claims. Those arguments and that evidence is insufficient prove that any Accused 2Wire Product allocates memory "in accordance with a message received during an initialization of the transceiver," as required by claim 19 of the '473 patent.

First, Dr. Cooklev's opinions relating to G.993.2 do not establish that this element of claim 19 is met. Dr. Cooklev again argues that "the 'max_delay_octet$_{DS,0}$' field of the O-PMS message specifies the maximum number of bytes of memory that are available to be allocated to a deinterleaver." Cooklev Opening Rpt. ¶ 381; *id.* ¶ 382 ("max_delay_octet$_{DS,0}$ of the O-PMS message specifies the maximum number of bytes of memory that are available to be allocated to the deinterleaver of the 5031NV."). Dr. Cooklev also states that "[t]he *I* and *D* for LP_0 define the amount of memory used for the upstream interleaver according to the equation: delay_octet$_{US,0}$/2 = ($I_{US,0}$ – 1) × ($D_{US,0}$ – 1)/2 octets (i.e., bytes) of memory." *Id.* ¶ 383. Neither of Dr. Cooklev's assertions is correct. As discussed above, the delay_octet and max_delay_octet parameters set forth, respectively, the actual and maximum end-to-end ***delay***. From those parameters, the minimum amount of memory required to support the end-to-end delay can be determined. *See* G993.2 § 6.2.8 ("Each interleaver and each de-interleaver for each latency path requires at least (delay_octet$_{[DS/US],[0]}$/2) octets of memory to meet this delay."). It is undisputed that the O-PMS message parameters do not specify any allocation of memory; they specify delay.

Second, Dr. Cooklev's testing of the accused products does not establish the allocation of memory "in accordance with a message received during an initialization of the transceiver." As discussed above, Dr. Cooklev's tests do not establish anything more than that, in the operation of the Accused 2Wire Products, the end-to-end interleaver delay in the downstream or upstream direction (delay_octet) is less than the maximum allowed end-to-end interleaver delay

(maximum_delay_octet), as expected based upon the specifications G.993.2. *See, e.g.*, Jacobsen Decl. ¶¶ 240, 242, 306, 308. The tests do not indicate how much memory the accused products actually used for interleaving or deinterleaving to meet the specified end-to-end interleaver delay or that they even allocated memory between the interleaving function and deinterleaving function. *Id.* Given this, there is no evidence to suggest that any of the accused products allocated memory "in accordance with" any message received during initialization.

Third, Dr. Almeroth's source code analysis is not evidence that the Accused 2Wire Products allocate interleaver or deinterleaver memory "in accordance with a message received during an initialization of the transceiver." Again, Dr. Almeroth states that the each of the accused products [redacted] Almeroth Opening Rpt., Attachment H at 11. Taking this analysis, Dr. Cooklev concludes that [redacted] Walsh Decl., Ex. A ¶ 394. Again, this is incorrect. As Dr. Almeroth admitted at his deposition, those values do not allocate memory. 2/8/19 Almeroth Dep. Tr. at 196:10–18 (Dr. Almeroth admitting that [redacted]); Jacobsen Decl. ¶¶ 245, 311. Nor do they specify the number of bytes of memory actually used by an interleaver or deinterleaver. Thus, TQ Delta has not shown that the accused products allocate memory "in accordance with" a message received during initialization.

2. 2Wire Does Not Infringe Claim 19 Of The '473 Patent Because The Claim Can Only Be Infringed When The Product Is Used In A DSL Service Provider Network.

Claim 19 of the '473 patent recites "a memory, wherein the memory ***is allocated*** between the interleaving function and the deinterleaving function in accordance with a message ***received***

during an initialization of the transceiver. . . ." The claim language requires that the memory is allocated in accordance with a message received during an initialization process. A person of ordinary skill in the art ("POSITA") would understand that the memory cannot be allocated as recited in claim 19 until after the transceiver has received the O-PMS message, which requires the transceiver to be connected to a subscriber line with a VTU-O on the service provider's end of the line. *See* Jacobsen Decl. ¶¶ 250–51, 317. Therefore, the Accused 2Wire Products cannot infringe claim 19 when they are sold. *Id.* Accordingly, summary judgment of non-infringement is warranted for this reason as well.

C. The Accused Products Do Not Satisfy The "Allocating" Limitations Of Claim 5 Of The '381 Patent And Claim 13 Of The '882 Patent As Originally Issued.

The Court should grant summary judgment of non-infringement as to claim 5 of the '381 patent and claim 13 of the '882 patent because it is undisputed that the Accused 2Wire Products do not practice the limitations of "allocating a first number of bytes of the shared memory to the deinterleaver . . ." and "allocating a second number of bytes of the shared memory to the interleaver . . .," as the claims read when the patents issued.

TQ Delta seeks to prove infringement of these claims as modified by certificates of correction that the applicants procured from the Patent Office after issuance. These certificates of correction should be invalidated by the Court because the purported mistakes in the claims that the applicants "corrected" in the certificates of correction—changing "transmission" to "reception," and "received" to "transmitted"—were more than mere typographical or clerical errors. The certificates materially affected the scope or meaning of the patents, and, therefore, were improperly issued by the Patent Office. *See* MPEP § 1481.

"Invalidating a certificate of correction for impermissible broadening . . . requires proof of two elements: (1) the corrected claims are broader than the original claims; and (2) the

presence of the clerical or typographical error, or how to correct that error, is not clearly evident to one of skill in the art." *Cent. Admixture Pharmacy Servs., Inc. v. Advanced Cardiac Sols., P.C.*, 482 F.3d 1347, 1353 (Fed. Cir. 2007); *see also S.O.I.Tec Silicon On Insulator Techs., S.A. v. MEMC Elec. Materials, Inc.*, 745 F. Supp. 2d 489, 506 (D. Del. 2010).

Under element (1), "[t]o answer the question of whether a claim has been broadened through correction requires interpreting the old and new versions of that claim, and then determining whether the new version covers territory the old one did not." *Cent. Admixture*, 482 F.3d at 1347; *see also Tillotson, Ltd. v. Walbro Corp.*, 831 F.2d 1033, 1037 n.2 (Fed. Cir. 1987) ("A claim . . . is broader in scope than the original claims if it contains within its scope any conceivable apparatus or process which would not have infringed the original patent"). Here, there is no dispute that claim 5 of the '381 patent and claim 13 of the '882 patent as amended by the certificates of correction cover different subject matter than those claims as originally issued; thus, the amendments impermissibly broadened the claims. *See* Jacobsen Decl. ¶ 153. For example, a transceiver that allocates "a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ***transmission*** at a first data rate" (as amended) would not be the same as or within the scope of a transceiver that allocates "a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ***reception*** at a first data rate" (as issued). A POSITA would understand that a transceiver that did not infringe claim 5 of the '381 patent or claim 13 of the '882 patent as issued could nevertheless infringe claim 5 of the '381 patent or claim 13 of the '882 patent as modified by their respective certificates of correction. *Id.*

Under element (2), "[s]ection 255 does not preclude broadening corrections so long as

they are corrections of clerical or typographical mistakes and 'only where it is clearly evident from the specification, drawings, and prosecution history how the error should appropriately be corrected.' Put another way, the public must be provided with notice as to the scope of the claims." *S.O.I.Tec*, 745 F. Supp. 2d at 506 (quoting *Superior Fireplace Co. v. Majestic Prod. Co.*, 270 F.3d 1358, 1372 (Fed. Cir. 2001)). A POSITA would not understand the applicant's original use of the terms "transmission" and "received" in claim 5 of the '381 patent and claim 13 of the '882 patent to be typographical errors. *See* Jacobsen Decl. ¶¶ 148–152. Setting aside the correction from "shred" memory to "shared" memory, which *is* a typographical error, a POSITA could read and understand the claims as originally written. *Id.* ¶ 148. It would not have been evident to a POSITA reading the claims, the specification, and the prosecution history of the patents that the original use of "transmission" and "received" was wrong or otherwise improper. *Id.* Indeed, the Examiner, who is presumed to be a person of ordinary skill in the art, *see In re Sang Su Lee*, 277 F.3d 1338, 1345 (Fed. Cir. 2002), examined these two patents as well as two other patents in the family and allowed the claims to issue each time with these supposed errors. *See* Jacobsen Decl. ¶¶ 149–51. It was not until the applicants sought post-issuance correction were these errors raised for the first time.

Once the improper certificates of correction are invalidated, as they should be, 2Wire is entitled to summary judgment of non-infringement of these claims. TQ Delta has produced no evidence that 2Wire infringes the claims as they issued.

VI. CONCLUSION

For the reasons stated above, 2Wire respectfully requests that the Court grant summary judgment of non-infringement of the asserted claims of the Family 3 patents.

Dated: February 22, 2019

Respectfully submitted,

/s/ Jody C. Barillare

Jody C. Barillare (#5107)
MORGAN LEWIS & BOCKIUS LLP
The Nemours Building
1007 North Orange Street, Suite 501
Wilmington, Delaware 19801
Telephone: 302.574.3000
Facsimile: 302.574.3001
jody.barillare@morganlewis.com

Brett Schuman (*pro hac vice*)
Rachel M. Walsh (*pro hac vice*)
Monte M.F. Cooper (*pro hac vice*)
GOODWIN PROCTER LLP
Three Embarcadero Center, 24th Floor
San Francisco, California 94111
Telephone: 415.733.6000
Facsimile: 415.677.9041
bschuman@goodwinprocter.com
rwalsh@goodwinprocter.com
mcooper@goodwinlaw.com